## Republic of Iraq The Ministry of Higher Education & Scientific Research



University: Hamdaniya College: Education Department: Computer Science Stage: First Subject: Logic Design

## **Course Weekly Outline**

Week	Date	Topics Covered	Lab. Experiment Assignments	Notes
1		1- Numbers SYSTEMS		
		decimal Number		
		Binary Number		
		Octal Number		
		Hexadecimal Number		
2		2- Conversions between system		
		1-2-1 decimal to Binary Conversion		
		1-2-2 Binary to decimal Conversion		
		1-2-3 decimal to Octal Conversion		
		1-2-4 Octal to decimal Conversion		
		1-2-5 decimal to Hexadecimal Conversion		
3		1-2-6 Hexadecimal to decimal Conversion		
		1-2-7 Binary to Octal Conversion		
		1-2-8 Octal d to Binary Conversion		
		1-2-9 Binary to Hexadecimal Conversion		
		1-2-10 Hexadecimal to Binary Conversion		
		1-2-11 Octal d to Hexadecimal Conversion 1-		
		2-12 Hexadecimal to Octal Conversion		
4		1-3 Arithmetic Operations 1-3-		
		1 Addition		
		Addition in Binary		
		Addition in Octal		
		Addition in Hexadecimal		

5	1-3-2 Complements
	1's Complements In Binary
	2's Complements In Binary
	1's and 2's Complements in decimal
	1's and 2's Complements in Octal
	1's and 2's Complements in Heyadecimal
	i s and 2 s complements in recadecimat
6	1-3-3 Subtraction in Binary
	1-3-4 Multiplication in Binary 1-3-4
	Division in Binary
7	Signed Number
1	Signed Number
	2-1 Binary coded decimal(BCD)
	2-2 Encess 3
	2-3 The Grav code
	2-4 parity binary number
	2-4-1 odd-parity
8	3 Boolean Algebra
	3-1 Boolean Operations
	3-2 Rules and laws of Boolean algebra
	<ul> <li>3.3 Standard Barrasantation for Logical</li> </ul>
	3-3-1 The SOP and The POS
9	3-4 The Karnaugh Map
	3-4-1 Two –variable The Karnaugh Map
	3-4-2 Three –variable The Karnaugh Man
	3.4.3 four variable The Karnaugh Man
	5-4-5 four -variable the Karnaugh Map
	3-4-4simplification Karnaugh Map
	3-4-5don't care condition
	3-5 Design Examples
10	
10	3-5-1 Half-adder
	3-5-2 Full adder
	3-5-3 Half subtractor
	3-5-4 Full Subtractor
	3-3-3 BCD 10 /_ SEGMENT

11		DECODER						
		3-5-6Convert cray to binary						
		3-5-7 Convert binary to cray						
		3-5-8 Parallel adder circuit						
Half-year Break								
17								
1/		4 Flip-Flops						
		4-1 Flip Flops R-S						
		4-2 Fup-Flops K-5 laten 4-3D-type flin-flop						
		4 - 4 J - k = Flin Flon						
		4-5 TOGGLE FF(T-FF)						
10								
18		5 Encoder and Decoder						
10								
19		6 Multiplexers and their use in combinational logic design						
20								
20		7 Read Only Memory (ROM)						
01								
21		8 Counters 8-1Parallel counter						
		8-20ther counter						
22		0 Shift Degistars						
22		9-Sint Registers 9-1Introduction						
		9-2Serial Shift Registers						
		9-3Parallel Shift Registers						
	1							

Instructor Signature:

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